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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,448	09/16/2003	Georg Muller	BGJ-102	1586

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EXAMINER	
CHAN, EMILY Y	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 03/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/663,448	MULLER, GEORG
	Examiner	Art Unit
	Emily Y. Chan	2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) *13-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2-11-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's election with traverse of traverse in the reply filed on 1-18-05 is acknowledged. The traversal is on the ground(s) that there would not be any serious burden on the examiner to examine all the claims in the application including the apparatus. This is not found persuasive because the method claims recite the step of determining a voltage dropping over the pull-up and/or pull –down circuit and determine a total impedance of the pull-up and pull-down circuit are not recited in the apparatus claims 13-16 whereas the apparatus claims recite a test mode circuit and at least one semiconductor device to be tested by the testing apparatus are not required in the method claims 1-12. The examiner has to search the impedance and voltage determining for the method claims which are not required for examining the apparatus claims and has to search the test mode circuit and device to be tested for the apparatus claims which are not required for examining the method claims. Therefore, the requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raychaudhuri US publication 2003/0025535 in view of Sim US patent No. 5438545.

With respect to claim 1, Raychaudhuri ('535) disclose a method (see Figs 3-4) for measuring the impedance of driver devices provided in a semiconductor device, wherein a device (output driver) including a pull-up circuit (10) and a pull-down circuit (12) is used, the method comprising :

joint activating of both the pull-up circuit and the pull-down circuit and joint de-activating both the pull-up circuit (10) and the pull-down circuit (12) (see Fig. 3b);

Raychaudhuri ('535) does not disclose the step of determining a first current flowing through the pull-up circuit or the pull-down circuit.

Sim ('545) discloses a data output driver (see Fig. 3) comprising a pull-up circuit (I4) and a pull-down circuit (I10). Sim ('545) particularly teaches for determining a first current flow through a pull-down circuit (I10), with jointly activated pull-up and pull-down circuit (see Abstract, lines 4-6).

It would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to incorporate the step of determining the current flow through the pull-down circuit as taught by Sim ('545) into Raychaudhuri ('535)'s system so that Raychaudhuri ('535)'s system can perform the current determination on the pull-down circuit because Sim ('545) discloses that sensing and adjusting the current of the data output driver can prevent noises from occurring in chips (see Col. 5, lines 15-16).

With respect to claims 2-4, Sim ('545) does not specify to determine a standby current flowing between the supply voltage and the ground for claim 2, to determine a total current flowing between the supply voltage pad and the ground for claim 3 and to determine the first current by deducting the standby current from the total current for

claims 4. However, to determine the total current or standby current as claimed would be considered to be functionally equivalent to the current flow through the pull-down circuit determination of Sim ('545) because they are all directed to the same purpose of determining the current flow in the driver device and where to determine the current flow depends on its application of the device (see MPEP 2144.06 "Art Recognized Equivalence for the Same Purpose"). Therefore, the recited steps for determining the standby current and the total current would have been obvious to one of skilled in the art in view of Sim ('545)'s teaching of determining the current flowing into the pull-down circuit.

With respect to claims 5-6, Raychaudhuri ('535) discloses determining a voltage dropping over the pull-up and/or pull-down circuit, in particular with jointly activated pull-up and pull-down circuits (see Fig. 4, 40 and page 4, paragraph 0057, last lines 5-6).

With respect to claim 7, Raychaudhuri ('535) discloses that the method steps are performed several times in sequence, each with different settings of transistors contained in the pull-up or pull down circuit (see page 4, paragraphs 0052-0055).

With respect to claims 8-9, Raychaudhuri ('535) discloses the step of determining a total impedance of the pull-up and pull-down circuit (see page 4, paragraph 0051, lines 4-5) and a voltage dropping over the pull-up and/or pull-down circuit as determined.

With respect to claim 10, Raychaudhuri ('535) discloses that the device is a driver device (output driver) used for the driving of output signals during the regular operation of the semiconductor device (integrated circuit).

With respect to claim 11, Raychaudhuri ('535) discloses that a test device (impedance control circuit 22) is a test device not used for the driving of output signals during the regular operation of the semiconductor device.

With respect to claim 12, Raychaudhuri ('535) discloses that the test device (impedance control circuit 22) is connected with a device (dummy circuit 32) provided on the semiconductor device (integrated circuit)itself, by means (40) of which a voltage dropping over the pull-up and/or pull-down circuit is determined.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tomasetti et al US patent No. 5,338,987 discloses BiCMOS output driver (see Fig. 2) for transceiver circuit comprising pull-up circuit (14) , a pull-down circuit (17) and a driver control circuit (20) .

Ho et al US patent No.6,281,719 disclose an output pad precharge circuit (see Fig.3) comprising a pull-up circuit (70), a pull-down circuit (71), control signals for activating the pull-up circuit (70) and a pull-down circuit (71).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emily Y. Chan whose telephone number is 571-272-1956. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on 571-272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC
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PRIMARY EXAMINER
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03/07/05